# EXHIBIT H

**Analysis of Infringement of U.S. Patent No. 6,660,651 by Silicon Laboratories Inc.**
**(Based on Public Information Only)**

Plaintiff Ocean Semiconductor LLC ("Ocean Semiconductor"), provides this preliminary and exemplary infringement analysis with respect to infringement of U.S. Patent No. 6,660,651, entitled "ADJUSTABLE WAFER STAGE, AND A METHOD AND SYSTEM FOR PERFORMING PROCESS OPERATIONS USING SAME" (the "'651 patent") by Silicon Laboratories Inc. ("SILABS"). The following chart illustrates an exemplary analysis regarding infringement by Defendant SILABS's semiconductor products, systems, devices, components, integrated circuits, and products containing such circuits, fabricated or manufactured using ASML's semiconductor fabrication or manufacturing equipment and/or platforms (e.g., ASML's TWINSCAN system). Such products include, without limitation, wireless products (e.g., EFR32XG2X family), internet of things products (e.g., EFM8BB10F8G-QFN20, EFM8BB10F2A-QFN20, EFM8BB10F2G-QFN20, EFM8BB10F2I-QFN20, EFM8BB10F4A-QFN20, EFM8BB10F4G-QFN20, EFM8BB10F4I-QFN20, EFM8BB10F8A-QFN20, EFM8BB10F8G-QSOP24, EFM8BB10F8G-SOIC16, EFM8BB10F8I-QFN20, EFM8BB10F8I-QSOP24, EFM8BB10F8I-SOIC16, EFM8BB21F16A-QFN20, EFM8BB21F16G-QFN20, EFM8BB21F16G-QSOP24, EFM8BB21F16I-QFN20, EFM8BB21F16I-QSOP24, EFM8BB22F16A-QFN28, EFM8BB22F16G-QFN28, EFM8BB22F16I-QFN28, EFM8BB31F16A-4QFN24, EFM8BB31F16A-5QFN32, EFM8BB31F16G-QFN24, EFM8BB31F16G-QFN32, EFM8BB31F16G-QFP32, EFM8BB31F16G-QSOP24, EFM8BB31F16I-4QFN24, EFM8BB31F16I-5QFN32, EFM8BB31F16I-QFN24, EFM8BB31F16I-QFN32, EFM8BB31F16I-QFP32, EFM8BB31F16I-QSOP24, EFM8BB31F32A-4QFN24, EFM8BB31F32A-5QFN32, EFM8BB31F32G-QFN24, EFM8BB31F32G-QFN32, EFM8BB31F32G-QFP32, EFM8BB31F32G-QSOP24, EFM8BB31F32I-4QFN24, EFM8BB31F32I-5QFN32, EFM8BB31F32I-QFN24, EFM8BB31F32I-QFN32, EFM8BB31F32I-QFP32, EFM8BB31F32I-QSOP24, EFM8BB31F64A-4QFN24, EFM8BB31F64A-5QFN32, EFM8BB31F64G-QFN24, EFM8BB31F64G-QFN32, EFM8BB31F64G-QFP32, EFM8BB31F64G-QSOP24, EFM8BB31F64I-4QFN24, EFM8BB31F64I-5QFN32, EFM8BB31F64I-QFN24, EFM8BB31F64I-QFN32, EFM8BB31F64I-QFP32, EFM8BB31F64I-QSOP24), infrastructure products (e.g., Si5332A-GM1, Si5332A-GM2, Si5332A-GM3, Si5332B-GM1, Si5332B-GM2, Si5332B-GM3, Si5332C-GM1, Si5332C-GM2, Si5332C-GM3, Si5332D-GM1, Si5332D-GM2, Si5332D-GM3, Si5332E-GM1, Si5332E-GM2, Si5332E-GM3, Si5332F-GM1, Si5332F-GM2, Si5332F-GM3, Si5332G-GM1, Si5332G-GM2, Si5332G-GM3, Si5332H-GM1, Si5332H-GM2, Si5332H-GM3, Si5332A-GM1, Si5332A-GM2, Si5332A-GM3, Si5332B-GM1, Si5332B-GM2, Si5332B-GM3, Si5332C-GM1, Si5332C-GM2, Si5332C-GM3, Si5332D-GM1, Si5332D-GM2, Si5332D-GM3, Si5332E-GM1, Si5332E-GM2, Si5332E-GM3, Si5332F-GM1, Si5332F-GM2, Si5332F-GM3, Si5332G-GM1, Si5332G-GM2, Si5332G-GM3, Si5332H-GM1, Si5332H-GM2, Si5332H-GM3), broadcast products (e.g., Si2160, Si2162, Si2164, Si2180, Si2181, Si2182, Si2183), access products (e.g., Si3000, Si3402-GM, Si3404-GM, Si3406-GM, Si34062-GM, Si3462-GM, Si3471A-IM, microcontrollers (e.g., Tiny Gecko series, EFM8 Busy Bee), buffers (e.g., Si5330x), oscillators (e.g., Si54x), clock generators (e.g., Si534x), jitter attenuators (e.g., Si539x), synchronous ethernet (e.g., Si5383/48/88), isolation products (e.g., Si86xx, Si87xx, Si88xx, Si823x, Si827x, Si828x, Si823Hx, Si890x, Si892x, Si82Hx, Si838x, Si834x, and Si875x), interface products (e.g., ethernet controllers, LC controllers, bridges), timing products (e.g., buffers, clock generators, oscillators, and network synchronizers), sensors (e.g., humidity, magnetic, optical, temperature, and biometric), audio & radio products (e.g., automotive tuners, and radios), power products (e.g., power management ICs, powered drivers, and PSE

controllers), TV & video products (e.g., digital demodulators and TV tuners), modem & DAA products (e.g., voice modems), voice products (e.g., codec, proSLICs, and DAA), power over ethernet devices (e.g., power source equipment and powered device ICs)), and similar systems, products, devices, and integrated circuits ("'651 Infringing Instrumentalities").

The analysis set forth below is based only upon information from publicly available resources regarding the '651 Infringing Instrumentalities, as SILABS has not yet provided any non-public information.

Unless otherwise noted, Ocean Semiconductor contends that SILABS directly infringes the '651 patent in violation of 35 U.S.C. § 271(g) by using, selling, and/or offering to sell in the United States, and/or importing into the United States, the '651 Infringing Instrumentalities. The following exemplary analysis demonstrates that infringement. Unless otherwise noted, Ocean Semiconductor further contends that the evidence below supports a finding of indirect infringement under 35 U.S.C. § 271(b) in conjunction with other evidence of liability.

Unless otherwise noted, Ocean Semiconductor believes and contends that each element of each claim asserted herein is literally met through SILABS's provision or importation of the '651 Infringing Instrumentalities. However, to the extent that SILABS attempts to allege that any asserted claim element is not literally met, Ocean Semiconductor believes and contends that such elements are met under the doctrine of equivalents. More specifically, in its investigation and analysis of the '651 Infringing Instrumentalities, Ocean Semiconductor did not identify any substantial differences between the elements of the patent claims and the corresponding features of the '651 Infringing Instrumentalities, as set forth herein. In each instance, the identified feature of the '651 Infringing Instrumentalities performs at least substantially the same function in substantially the same way to achieve substantially the same result as the corresponding claim element.

Ocean Semiconductor notes that the present claim chart and analysis are necessarily preliminary in that Ocean Semiconductor has not obtained substantial discovery from SILABS nor has SILABS disclosed any detailed analysis for its non-infringement position, if any. Further, Ocean Semiconductor does not have the benefit of claim construction or expert discovery. Ocean Semiconductor reserves the right to supplement and/or amend the positions taken in this preliminary and exemplary infringement analysis, including with respect to literal infringement and infringement under the doctrine of equivalents, if and when warranted by further information obtained by Ocean Semiconductor, including but not limited to information adduced through information exchanges between the parties, fact discovery, claim construction, expert discovery, and/or further analysis.

| USP No. 6,660,651 | Infringement by the '651 Accused Instrumentalities |
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| 19. A method, comprising: providing a process chamber comprised of a wafer stage, said wafer stage having a surface that is adjustable; | ASML's TWINSCAN system provides a process chamber comprised of a wafer stage, the wafer stage having a surface that is adjustable.<br><br>For example, the TWINSCAN system performs the method of providing a process chamber:<br><br>  <br><br>*See* ASML DUV Lithography Systems, *available at* https://www.asml.com/en/products/duv-lithography-systems/twinscan-nxt1980di (last visited Apr. 30 2019).<br><br>The process chamber can be used for wafer exposure during lithography: |

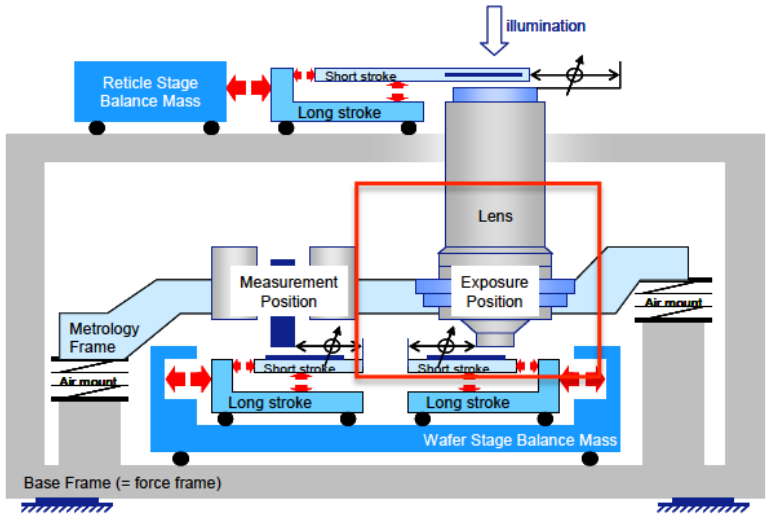


*Figure 5. TWINSCAN™ dynamic architecture*

*See* Perspective on Stage Dynamics and Control at 3.

The process chamber includes an adjustable wafer stage having a surface that is adjustable:

"In Figure 4, the table holding the wafer is called the mirror block because of the mirroring side surfaces, which allow interferometric position measurement (IFM)."

*See* Position Control at 31.

For example, the adjustable wafer stage or mirror block of the TWINSCAN system is shown below:

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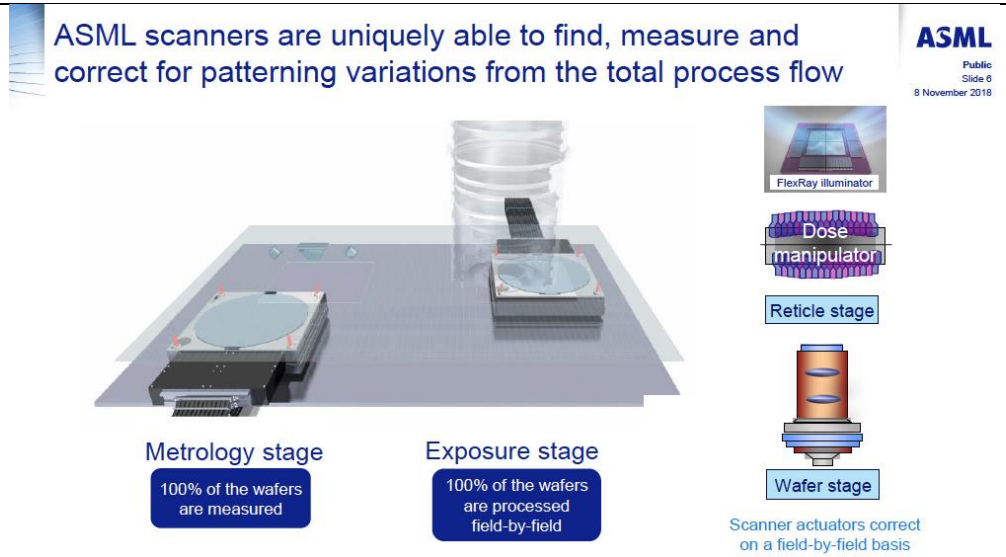
| |  <br>*See* Applications Products and Business Opportunity at 6. |
| adjusting said surface of said wafer stage by actuating at least one of a plurality of pneumatic cylinders that are operatively coupled to said wafer stage to accomplish at least one of raising, lowering and varying a tilt of said surface of said wafer stage; | ASML's TWINSCAN system adjusts the surface of the wafer stage by actuating at least one of a plurality of pneumatic cylinders that are operatively coupled to said wafer stage to accomplish at least one of raising, lowering and varying a tilt of said surface of said wafer stage.<br><br>For example, the TWINSCAN system adjusts the surface of the wafer stage by raising, lower, or tilting via wafer leveling using vertical actuators (e.g., in the "z direction"):<br><br>"Vertical actuators, which are mounted between the air foot and mirror block, allow the mirror block to be moved in z direction, as well as in rotational directions around the x and y axes, called x and $\Psi$, respectively."<br><br>*See* Position Control at 41; *see also id.* at 38 ("For wafer leveling, the actuators drive the mirror block with respect to the air foot, and hence vertical reaction forces can directly enter the silent, vibration-free, metro-frame world. Leveling now needs to be performed during scanning, making use of the wafer-height measurement by the level sensor.").<br><br>As another example, the TWINSCAN system actuates one of the six Lorentz actuators that are mounted between the air foot and the wafer stage to accomplish at least one of raising, lowering and varying a tilt of the surface of the wafer stage: |

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| | "Vertical actuators, which are mounted between the air foot and mirror block, allow the mirror block to be moved in z direction, as well as in rotational directions around the x and y axes, called x and $\Psi$, respectively."<br><br>*See* Position Control at 41.<br><br>Generally, the wafer stage is equipped with DOF Lorentz actuators (e.g., three DOF actuators for the horizontal directions and three DOF actuators for the vertical directions):<br><br>"The table also had vertical movement directions for the purpose of focusing the wafer in the image plane of the lens, requiring a measurement of the distance of the wafer to the lens by means of a level sensor system. The horizontal stage position was measured by an interferometer system. The stage was guided by means of mechanical bearings 'rolling' over the motor beams. With regard to controlling the stage, the horizontal controllers (3-DOF) acted independently from the vertical directions (also 3-DOF)."<br><br>*See* Perspective on Stage Dynamics and Control at 1.<br><br>As an example, for the x and y direction, the wafer table is adjusted by three Lorentz actuators such that the stage floats over a granite stone by means of an air bearing and the Lorentz actuators are connected to this granite stone: |

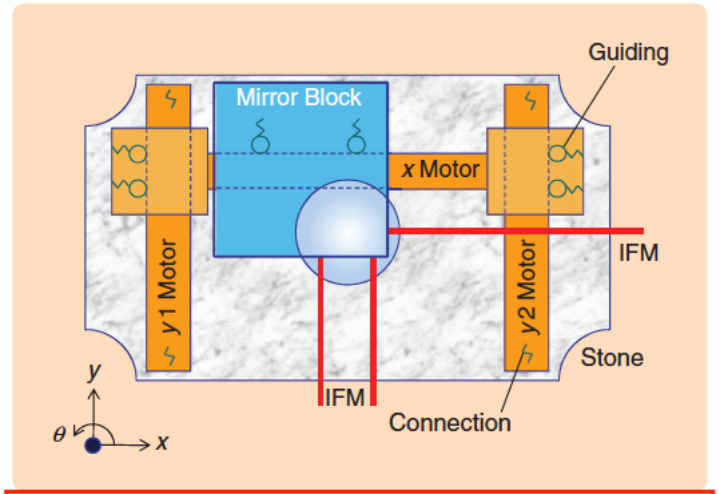


FIGURE 5 Wafer stage top view. The wafer table is driven by three actuators, two of which drive the stage in the *y* direction and the remaining one in the *x* direction. The linear actuators also function as a guide for the horizontal motion, cooperating with ball bearings in the mover. The stage floats over a granite stone by means of an air bearing, and the linear actuators are connected to this stone as well. Interferometers measure the stage position, making use of mirroring side surfaces of the stage.

*See* Position Control at 31.

In total, the TWINSCAN includes 6-DOF Lorentz actuators and 6-DOF stage control, in addition to offline leveling:

"In TWINSCAN™, a further perfection in the basic design was made by using balance masses, full 6-DOF Lorentz actuators and 6-DOF stage control, in addition to off-line levelling."

*See* Perspective on Stage Dynamics and Control at 3.

As another example, the vertical directions of the wafer stage can be achieved using Lorentz actuators:

"To avoid vibrations entering the mirror block, a Lorentz actuator is now also used for vertical directions, providing isolation in these directions as well. Because the required vertical range is smaller than 1 mm, no separate long-stroke motor is required. A 6DOF Lorentz-actuated block is the result"

*See* Position Control at 40.

A diagram showing the vertical connection that facilitates the vertical movement of the wafer stage is shown below:

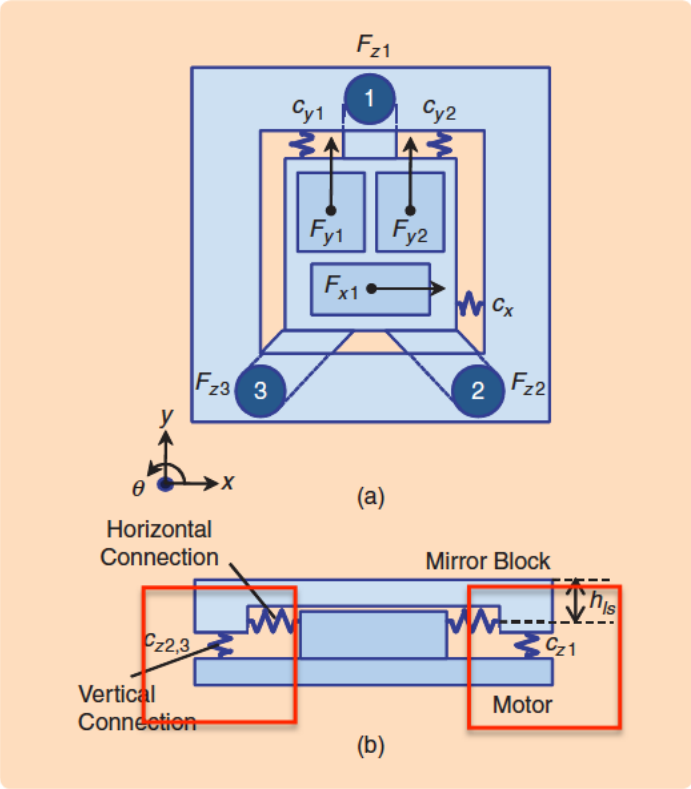


FIGURE 26 Stage layout with motor connection stiffness. The motor

*See* Position Control at 41 (annotated).

In one example, the wafer stage rotates around the center of the lens above it in the vertical directions using the actuators:

"The stage now rotates around the lens center instead of its center of mass. Especially in the vertical directions, the applicable rotations may show a high acceleration, depending on the vertical topology of the wafer surface."

*See* Position Control at 42.

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| | The wafer stage can also be tilted to help keep the wafer in focus:<br><br>"The reason for this lies in the scanning levelling: when the stage has to tilt around a horizontal axis to keep the wafer in focus, the stage tends to rotate around its center of mass, introducing a horizontal shift on wafer level."<br><br>*See* Perspective on Stage Dynamics and Control at 2. |
| positioning a wafer on said wafer stage; and | ASML's TWINSCAN system positions a wafer on the wafer stage.<br><br>For example, the TWINSCAN system positions the wafer on the wafer stage:<br><br>"After stepping the wafer to a new position, the wafer stage is allowed to wait until its position has settled such that the remaining error is sufficiently low before switching on the illuminating light. The MA and MSD after the step motion indicate the usability of the system for imaging."<br><br>*See* Position Control at 35.<br><br>The wafer is also loaded onto the wafer stage so that exposure can start:<br><br>"At the second stage, the wafer is loaded, and its surface is mapped in horizontal and vertical planes with respect to the stage itself. After the stage swap, the stage that is now positioned under the projection lens is aligned to the reticle in 6DOF by means of a through-the-lens optical system. With the wafer surface position known with respect to the stage and the stage position known with respect to the reticle, exposure can start."<br><br>*See* Position Control at 40. |
| performing a process operation on said wafer positioned on said wafer stage. | ASML's TWINSCAN system performs a process operation on the wafer position on the wafer stage.<br><br>For example, the TWINSCAN system performs stepper imaging or double patterning as part of the step-and-scan in exposing a wafer:<br><br>"After stepping the wafer to a new position, the wafer stage is allowed to wait until its position has settled such that the remaining error is sufficiently low before switching on the illuminating light. The MA and MSD after the step motion indicate the usability of the system for imaging."<br><br>*See* Position Control at 35. |

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| | Once the wafer is loaded, and its surface is mapped in horizontal and vertical planes with respect to the stage itself, the stage positioned under the projection lens is aligned to the reticle by means of a through-the-lens optical system. With the wafer surface position known with respect to the stage and the stage position known with respect to the reticle, exposure can start:<br><br>"Stage position measurement is now performed in all degrees of freedom by interferometers, with reference beams directed at the projection lens. This method provides a direct relative measurement of the position with respect to the lens. At the second stage, the wafer is loaded, and its surface is mapped in horizontal and vertical planes with respect to the stage itself. After the stage swap, the stage that is now positioned under the projection lens is aligned to the reticle in 6DOF by means of a through-the-lens optical system. With the wafer surface position known with respect to the stage and the stage position known with respect to the reticle, exposure can start."<br><br>*See* Position Control at 40. |